

Application No.: 10/630,642

Docket No.: JCLA8556-D

**REMARKS****Present Status of the Application**

The Office has rejected claims 14-15 and 20-21 under 35 U.S.C. 103(a) as being unpatentable over Applicants Admitted Prior Art (AAPA, Page 2 of the Specification and Figure 6) in view of Lebowitz (US 4,694,561, hereinafter "Lebowitz") in the Office Action mailed on January 30, 2006.

Applicants respectfully traverse the rejections addressed to claims 14-15 and 20-21 for at least the reasons set forth below. After carefully considering the remarks set forth in this Office Action and the cited references, Applicants respectfully submit that the presently pending claims are in condition for allowance. Reconsideration and withdrawal of the Examiner's rejection are requested.

**Response to 35 USC 103 Rejection**

*The Office Action has rejected claims 14-15 and 20-21 under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Lebowitz (US 4,694,561, hereinafter "Lebowitz").*

Applicants respectfully traverse the above rejections as set forth below.

The present invention, as basically recited in claim 14, teaches the following: "...removing a portion of the first type ion-doped well to form at least one first opening without exposing the

Application No.: 10/630,642

Docket No.: JCLA8556-D

first type ion-doped buried layer; and forming a second type ion-doped region in the first type ion-doped well at the bottom of the first opening”.

The Office alleges that Lebowitz teaches the trench capacitor, and it is thus obvious to one of ordinary skill in the art to modify the variable capacitor as disclosed by AAPA by forming the capacitor in the bottom of an opening as taught by Lebowitz. Applicants respectfully disagree with the Office’s assertions based on the following traversal:

ARGUMENT # 1

The federal circuit court had consistently held that a person of ordinary skill in the art must not only have had some motivation to combine the prior art teachings, but some motivation to combine the prior art teachings in the **particular manner claimed**. See, e.g., In re Kotzab, 217 F.3d 1365, 1371 (Fed. Cir. 2000)

“Particular findings must be made as to the reason the skilled artisan, with no knowledge of the claimed invention, would have selected these components for combination in the manner claimed.”; In re Rouffet, 149 F.3d 1350, 1357 (Fed. Cir. 1998)

“In other words, the examiner must show reasons that the skilled artisan, confronted with the same problems as the inventor and with no knowledge of the claimed invention, would select the elements from the cited prior art references for combination in the manner claimed.”

The Examiner argued that “[i]n response to applicant’s argument that the Lebowitz reference and Applicants’ Admitted prior art pertain to different problems, the fact that applicant has recognized another advantage would flow naturally from following the suggestion of the

Application No.: 10/630,642

Docket No.: JCLA8556-D

prior art cannot be the basis for patentability when the differences would otherwise be obvious..." on page 5 of the Office Action.

However, "in the manner claimed" is based upon the claimed invention having at least one specific, substantial, and credible utility for satisfying the criteria under 35 U.S.C. 101. Therefore, "in the manner claimed" is consistent with "the objective of the invention". In other words, "in the manner claimed" fulfills the utility requirement described in MPEP 706.03(a).

On the other hand, the Examiner has mistaken the above facts as arguments for "ADDITIONAL ADVANTAGES OR LATENT PROPERTIES" as described in MPEP 2145, which is clearly not the case.

The fact that the present invention may have additional advantages besides the aforementioned claimed specific, substantial, and credible utility is not the main issue for contention. The Applicants are not arguing based upon "additional advantages or latent properties" of the claimed invention, but are instead, traversing based upon "in the manner claimed", which is in accordance to the specific, substantial, and credible statutory utility requirement and "objective" of the present invention. A comparison of a claimed objective in accordance with statutory utility requirement to be made with respect to a mere "additional advantage" of an invention is not therefore a valid comparison done on the same footing.

Thus, the problem to be solved of the present invention is to provide a high-frequency variable capacitor having a considerably smaller resistance occupying a smaller space. Lebowitz, on the other hand, is directed at providing a method for fabricating a VLSI DRAM array of the

Application No.: 10/630,642

Docket No.: JCLA8556-D

type whose memory cells include Hi-C trench capacitors as described in col. 2, lines 13-18 in Lebowitz.

ARGUMENT # 2

According to MPEP 2142, “[t]o establish a **prima facie** case of obviousness, three **basic criteria must be met**. First, there must be some **suggestion or motivation**, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to **combine reference teachings**.” As a result, the following facts are highly relevant in establishing evidence of whether or not there were any suggestions in the knowledge generally available to one of ordinary skill in the art to combine the reference teachings, as contrary to the remarks by the Examiner in the Office Action on page 5.

The key question at hand is whether a person skilled in the art when faced with the problem of providing a variable capacitor having a considerably smaller resistance occupying a smaller space would be obvious to select AAPA and Lebowitz, and to modify the variable capacitor as disclosed by AAPA by forming the capacitor in the bottom of an opening as taught by Lebowitz based upon the know-how during the time that the invention was made?

To try to answer the above key question, we had accomplished the following:

Using keywords such as “variable capacitor”, “improved resistance”, “Q”, and “small space”, “quality factor”, and “high-frequency” together as well as various obvious variants of the aforementioned keywords (which are consistent with the objective of the present invention),

Application No.: 10/630,642

Docket No.: JCLA8556-D

searches were conducted using the USPTO Published Applications (AppFT), Issued Patents (PatFT) system, and the internet. The following are the search results:

**Search Results using Google**

1. [http://www-bsac.eecs.berkeley.edu/archive/masters/patrick\\_riehl\\_ms.pdf](http://www-bsac.eecs.berkeley.edu/archive/masters/patrick_riehl_ms.pdf) [Micromachining of MEMS devices for producing variable capacitor that uses a vertical resonator]
2. [http://www.eng.yale.edu/qlab/papers/reprints/JS\\_supercurrent.pdf](http://www.eng.yale.edu/qlab/papers/reprints/JS_supercurrent.pdf)  
[Capacitor made using plates made of Au, resistors of an AuCu alloy, and Al-AlOx-Al Josephson junctions] 1999
3. [http://mems.colorado.edu/c1.gen.prjct/DARPA\\_fame/](http://mems.colorado.edu/c1.gen.prjct/DARPA_fame/)  
[Chemical approach for improving properties of ferroelectric materials. And physical approach to control the gap or area of the dielectric layer via MEMS]
4. <http://kabuki.eecs.berkeley.edu/~gabed/245finalreport.pdf>  
[MEMS – tunable parallel plate air-gap capacitor and suspended movable plates MEMS typed variable capacitor]
5. [http://en.wikipedia.org/wiki/Practical\\_capacitors#Variable\\_capacitors](http://en.wikipedia.org/wiki/Practical_capacitors#Variable_capacitors)  
[Improving via large junction area and doping profile]

**USPTO Published Applications (AppFT) and Issued Patents (PatFT) search results**

1. US – 2002/0040991  
[Using metal-to-metal capacitors]

Application No.: 10/630,642

Docket No.: JCLA8556-D

2. US – 2002/0158717

[Semiconductor varactor is typically noisy and lossy, particularly in applications above 500 MHz, it is ineffective for high-frequency, low-loss applications – this reference **TEACHES AWAY FROM present invention**, and suggests using Ferroelectric tunable capacitors - ceramic rare-earth oxides.]

3. US – 6,885,263

[Ferroelectric tunable capacitors - ceramic rare-earth oxides]

[Semiconductor varactor is typically noisy and lossy, particularly in applications above 500 MHz, it is ineffective for high-frequency, low-loss applications – this reference **TEACHES AWAY FROM present invention**, and suggests using Ferroelectric tunable capacitors - ceramic rare-earth oxides.]

4. US-6,806,553

[Dielectric constant is changed by application of a control voltage, and dielectric layer - a plurality of capacitance-producing regions electrically connected to each other.]

5. US -6,661,069

[Comb-drive electrodes are used for actuation while control or signal electrodes sense the motion of the movable electrode – MEMS.]

6. US-6,642,607

[Layers of different conductivities where one layer is epitaxially grown on another. A PN junction region is serving as a variable capacitance between the layers.]

Application No.: 10/630,642

Docket No.: JCLA8556-D

Based upon the above results, it is **evident that the answer to the key question** of “whether a person skilled in the art when faced with the problem of providing a variable capacitor having a considerably smaller resistance occupying a smaller space for high-frequency application would be obvious to use AAPA and Lebowitz, **and to modify the variable capacitor as disclosed by AAPA by forming the capacitor in the bottom of an opening as taught by Lebowitz based upon the know-how up to the time that the invention was made ?” should be have been NO.**

### ARGUMENT # 3

The Examiner has asserted that the recitation “variable capacitor” has not been given patentable weight because the recitation occurs in the preamble on page 5 of the Office Action.

A specific and substantial utility, as described in MPEP 2107, of the present invention required for the compliance of the utility requirements of 35 U.S.C. 101 and 112, first paragraph, described in MPEP 2107, is found specifically with the “providing a **variable capacitor** having a considerably smaller resistance occupying a smaller space”. This is fully supported in Paragraphs [0007]-[0008] of the present invention.

In other words, the inclusion of “variable capacitor” as a claim limitation is required for the providing for a specific and substantial utility for the present invention. Therefore, if the “variable capacitor” were removed from Claim 14, for example, as a claim limitation, the remaining features and limitations by themselves together in Claim 14 are as shown as follows:

*comprising the steps of:*

Application No.: 10/630,642

Docket No.: JCLA8556-D

*providing a substrate having a first type ion-doped buried layer and a first type ion-doped well, wherein the first type ion-doped buried layer is above below and in connection to the first type ion-doped well;*

*forming a conductive layer in the substrate above the first type ion-doped buried layer;*

*removing a portion of the first type ion-doped well to form at least one first opening without exposing the first type ion-doped buried layer; and*

*forming a second type ion-doped region in the first type ion-doped well at the bottom of the first opening.*

Based upon the knowledge of a person skilled in the art, the above sets of limitations in Claim 14 could very well be interpreted as part of a definition of a diode, a transistor, etc..., and maybe not even of a variable capacitor because of the lacking of a relatively large collector found in conventional variable capacitors as shown in FIG. 6 of the present invention. In other words, the above traversal shows that the above sets of claim limitations by themselves in Claim 14 have clearly “non-specific” and/or “non-substantial” utilities. As a result, the above sets of limitations without the “variable capacitor” being used as a claim limitation would not yield a “specific and substantial utility” for fulfilling the UTILITY and/or ENABLEMENT requirements (as described in MPEP 2164) for the present invention, and would not be able to stand alone (without the “variable capacitor” as a limiting feature).



Application No.: 10/630,642

Docket No.: JCLA8556-D

As one can see that if suppose all of the corresponding support such as in paragraphs [0003], [0006], [0009] – [0012] of the present invention for the feature “variable capacitor” are not accorded any patentable weight, the specific and substantial UTILITY and/or ENABLEMENT requirements of 35 U.S.C. 101 and 112, respectively, would no longer be met. That is to say, the corresponding support in the description used during the claim construction of Claims 14 without any of the corresponding support dedicated for the feature “variable capacitor” shall no longer be able to support the specific and substantial UTILITY and/or ENABLEMENT requirements.

Therefore, the body of the Claim 14 clearly does depend on the “variable capacitor” in the preamble for completeness, and the process steps are not able to stand alone for the sake of compliance with the specific and substantial UTILITY and/or ENABLEMENT requirements of 35 U.S.C. 101 and 112, respectively.

Likewise, the body of the Claims 15, 20 and 21 depend on the “variable capacitor” in the preamble in Claim 14 for completeness as well, and the process steps are not able to stand alone for the sake of compliance with the UTILITY and/or ENABLEMENT requirements of 35 U.S.C. 101 and 112, respectively.

#### ARGUMENT # 4

Furthermore, would there be any suggestions or teachings in Lebowitz for specifically reducing the resistance of a variable capacitor by means of modifying the variable capacitor by forming capacitor in the bottom of an opening? It seems that Lebowitz only suggested or taught mainly the following: 1) high capacitance capacitor for a DRAM, 2) direct electrical connection

Application No.: 10/630,642

Docket No.: JCLA8556-D

between capacitor and adjacent transistor, 3) a high performance DRAM cell, and 4) achieving capacitance performance in a relatively small-surface-area using a trench. [Lebowitz, Abstract, and col .1, lines 6-65]

ARGUMENT # 5

Does Lebowitz contain any teachings that teaches away from the key point of contention, which is “modify variable capacitor by forming capacitor in the bottom of an opening”? The answer should be YES as supported in the following:

“In order to realize specified values of capacitance in relatively small-surface-area capacitors, proposals have been recently made for fabricating each cell capacitor as a vertical structure that extends into the substrate of the semiconductor chip in which the VLSI DRAM memory is formed. This so-called trench capacitor design has a major portion of its plates extending into rather than along the surface of the chip. The amount of surface area required per capacitor is only the area of the trench at the surface of the chip.” [Lebowitz, Col. 31-40] In other words, Lebowitz teaches a strategy of using vertical structures in the form of trenches for achieving improved capacitance performances instead.

In the Office Action dated January 30, 2006, the Examiner has alleged that “[i]n response to applicant’s argument that the references fail to show certain features of applicant’s invention, it is noted that the features upon which applicant relies (i.e., no presence of trench/opening) are not recited in the rejected claim(s).” as stated on page 6 of the Office Action.

Application No.: 10/630,642

Docket No.: JCLA8556-D

In response to the above, the following are the corresponding traversals: 1) claims typically require explicit features and limitations necessary to satisfy the statutory and form requirements relating to utility, claim scope, and particularly pointing out and claiming the invention, etc.; therefore, there is no actual requirement to include claim limitations for all of the many possible negative limitations, i.e. no presence of trench/opening; 2) the main question (instead of whether or not if there is any explicit feature of “no presence of trench/opening” in the claim) should be whether a person skilled in the art when interpreting Claim 14 would clearly understand that Claim 14 does not teach of “achieving capacitance performance in a relatively small-surface-area using a trench” as taught in Lebowitz; 3) claim limitations can be explicit as well as inherent as discussed in MPEP 2114; therefore, by virtue of Claim 14 teaching a different method of manufacturing variable capacitor, FIGs. 1A to 1D, 2A to 2E, 3A to 3F, 4A to 4G, and 5A to 5H of the present invention all inherently exclude the teachings of Lebowitz of “achieving capacitance performance in a relatively small-surface-area using a trench”.

Based upon the above arguments/traversing, we find that there are compelling evidence which supports the patentability of claims 14-15 and 20-21 for overcoming the 35 U.S.C. 103(a) rejections based on AAPA in view of Lebowitz.

As a result, claims 14-15, and 20-21 should be allowed.

Application No.: 10/630,642

Docket No.: JCLA8556-D

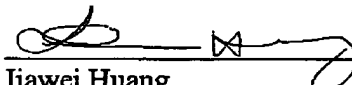
**CONCLUSION**

For at least the foregoing reasons, it is believed that the presently pending claims 14-27 of the present application patentably define over the prior art and are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Date: 3/27/2006

4 Venture, Suite 250  
Irvine, CA 92618  
Tel.: (949) 660-0761  
Fax: (949)-660-0809

Respectfully submitted,  
J.C. PATENTS

  
Jiawei Huang  
Registration No. 43,330